

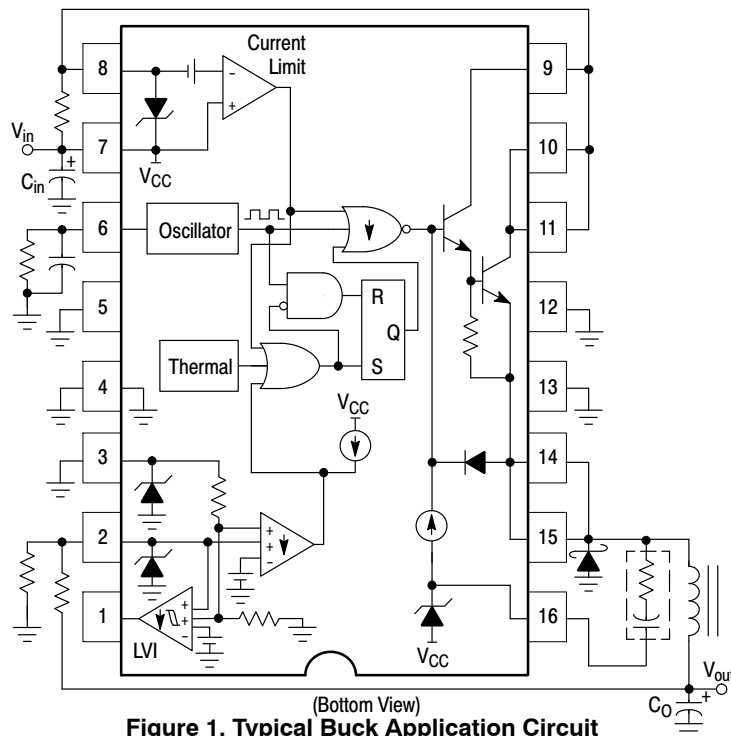
# NCP3163, NCV3163

## 3.4 A, Step-Up/Down/ Inverting 50-300 kHz Switching Regulator

The NCP3163 Series is a performance enhancement to the popular MC33163 and MC34163 monolithic DC-DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This controller was specifically designed to be incorporated in step-down, step-up, or voltage-inverting applications with a minimum number of external components. The NCP3163 comes in an exposed pad package which can greatly increase the power dissipation of the built in power switch.

### Features

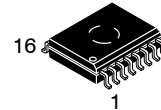
- Output Switch Current in Excess of 3.0 A
- 3.4 A Peak Switch Current
- Frequency is Adjustable from 50 kHz to 300 kHz
- Operation from 2.5 V to 40 V Input
- Externally Adjustable Operating Frequency
- Precision 2% Reference for Accurate Output Voltage Control
- Driver with Bootstrap Capability for Increased Efficiency
- Cycle-by-Cycle Current Limiting
- Internal Thermal Shutdown Protection
- Low Voltage Indicator Output for Direct Microprocessor Interface
- Exposed Pad Power Package
- Low Standby Current
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control
- These are Pb-Free Devices



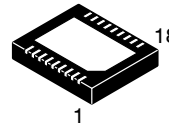
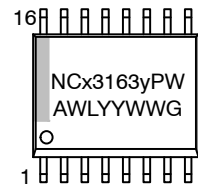
**ON Semiconductor®**

<http://onsemi.com>

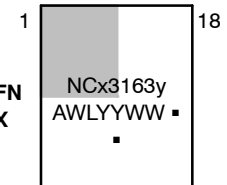
### MARKING DIAGRAMS



**SOIC-16W  
EXPOSED PAD  
PW SUFFIX  
CASE 751AG**



**18-LEAD DFN  
MN SUFFIX  
CASE 505**



NCx3163y = Specific Device Code  
 x = P or V  
 y = blank or B  
 A = Assembly Location  
 WL = Wafer Lot  
 YY = Year  
 WW = Work Week  
 G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 18 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NCP3163, NCV3163

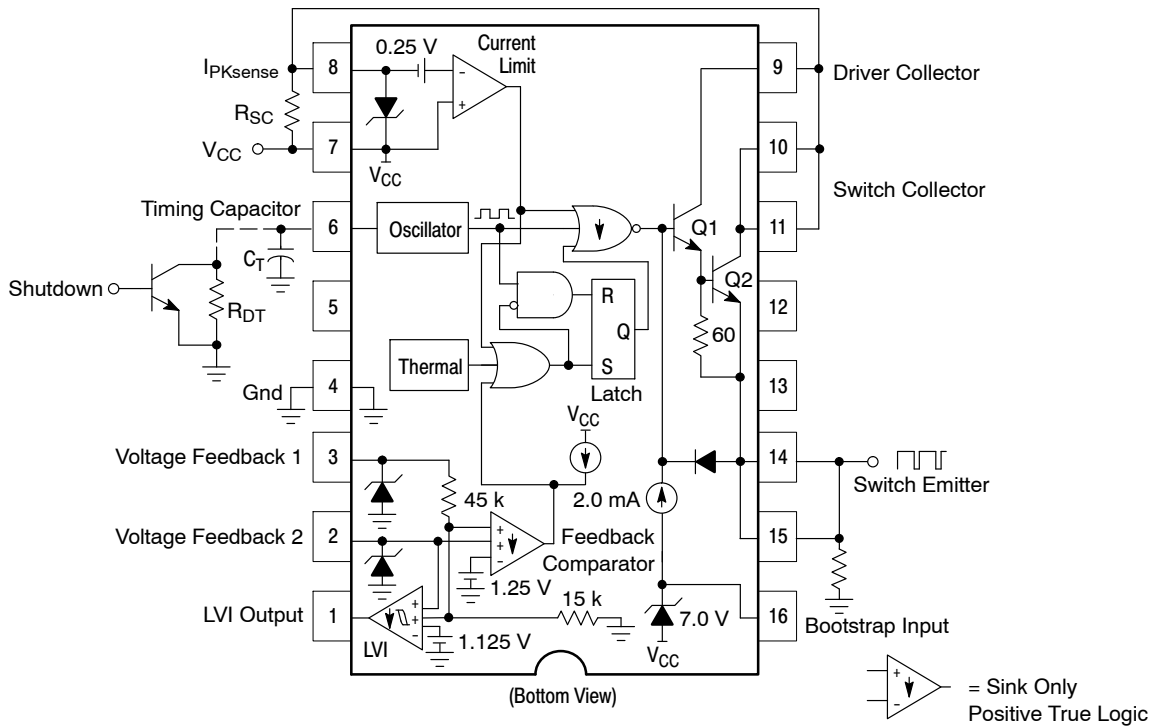


Figure 2. Representative Block Diagram

## PIN FUNCTION DESCRIPTION

| SOIC16      | DFN18       | PIN NAME           | DESCRIPTION  |
|-------------|-------------|--------------------|--|
| 1           | 15          | LVI Output         | This pin will sink current when FB1 and FB2 are less than the LVI threshold ( $V_{th}$ ).  |
| 2           | 16          | Voltage Feedback 2 | Connecting this pin to a resistor divider off of the output will regulate the application according to the $V_{out}$ design equation in Figure 22.   |
| 3           | 17          | Voltage Feedback 1 | Connecting this pin directly to the output will regulate the device to 5.05 V.   |
| 4           | 18          | GND                | Ground pin for all internal circuits and power switch.   |
| 6           | 1           | Timing Capacitor   | Connect a capacitor to this pin to set the frequency. The addition of a parallel resistor will decrease the maximum duty cycle and increase the frequency.   |
| 7           | 3           | $V_{CC}$           | Power pin for the IC.  |
| 8           | 4           | $I_{pk}$ Sense     | When $(V_{CC} - V_{IPKsense}) > 250$ mV the circuit resets the output driver on a pulse by pulse basis.  |
| 9           | 5           | Drive Collector    | Voltage driver collector   |
| 10,11       | 6,7,8,9     | Switch Collector   | Internal switch transistor collector   |
| 14,15       | 10,11,12,13 | Switch Emitter     | Internal switch transistor emitter   |
| 16          | 14          | Bootstrap Input    | Connect this pin to $V_{CC}$ for operation at low $V_{CC}$ levels. For some topologies, a series resistor and capacitor can be utilized to improve the converter efficiency.                               |
| 5,12,13     | 2           | No Connect         | These pins have no connection.   |
| Exposed Pad | Exposed Pad | Exposed Pad        | The exposed pad beneath the package must be connected to GND (pin 4). Additionally, using proper layout techniques, the exposed pad can greatly enhance the power dissipation capabilities of the NCP3163. |

# NCP3163, NCV3163

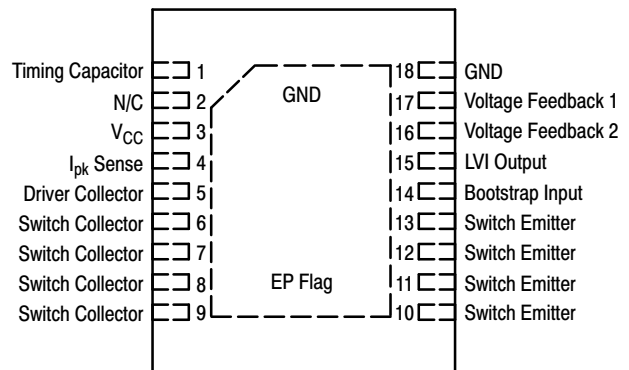
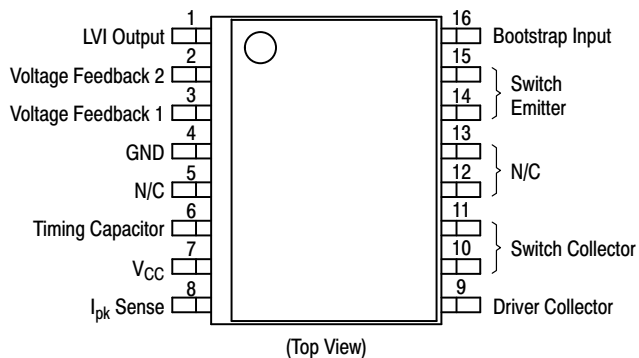
## MAXIMUM RATINGS (Note 1)

| Rating   | Symbol          | Value                                | Unit                        |
|--|-----------------|--------------------------------------|-----------------------------|
| Power Supply Voltage                                 | $V_{CC}$        | 0 to +40                             | V                           |
| Switch Collector Voltage Range                       | $V_{CSW}$       | -1.0 to +40                          | V                           |
| Switch Emitter Voltage Range                         | $V_{ESW}$       | -2.0 to +40                          | V                           |
| Switch Collector to Emitter Voltage                  | $V_{CESW}$      | +40                                  | V                           |
| Switch Current                                       | $I_{SW}$        | 3.4                                  | A                           |
| Driver Collector Voltage (Pin 8)                     | $V_{CC}$        | -1.0 to +40                          | V                           |
| Driver Collector Current (Pin 8)                     | $I_{CC}$        | 150                                  | mA                          |
| Bootstrap Input Current Range                        | $I_{BST}$       | -100 to +100                         | mA                          |
| Current Sense Input Voltage Range                    | $V_{IPKSNS}$    | $(V_{CC} - 7.0)$ to $(V_{CC} + 1.0)$ | V                           |
| Feedback and Timing Capacitor Input Voltage Range    | $V_{in}$        | -1.0 to +7.0                         | V                           |
| Low Voltage Indicator Output Voltage Range           | $V_{CLVI}$      | -1.0 to +40                          | V                           |
| Low Voltage Indicator Output Sink Current            | $I_{CLVI}$      | 10                                   | mA                          |
| <b>Power Dissipation and Thermal Characteristics</b> |                 |                                      |                             |
| Thermal Characteristics                              |                 |                                      | $^{\circ}\text{C}/\text{W}$ |
| Thermal Resistance, Junction-to-Case                 | $R_{\theta JC}$ | 15                                   |                             |
| Thermal Resistance, Junction-to-Air                  | $R_{\theta JA}$ | 56                                   |                             |
| Storage Temperature Range                            | $T_{stg}$       | -65 to +150                          | $^{\circ}\text{C}$          |
| Maximum Junction Temperature                         | $T_{Jmax}$      | +150                                 | $^{\circ}\text{C}$          |
| Operating Ambient Temperature (Note 3)               | $T_A$           |                                      | $^{\circ}\text{C}$          |
| NCP3163  |                 | 0 to +70                             |                             |
| NCP3163B   |                 | -40 to +85                           |                             |
| NCV3163  |                 | -40 to +125                          |                             |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- This device series contains ESD protection and exceeds the following tests:  
Human Body Model 2000 V per MIL-STD-883, Method 3015.  
Machine Model Method 200 V.  
Charged Device Model 750 V for corner pins and 500 V for others (according to AEC-Q100).
- This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78.
- Maximum package power dissipation limits must be observed. Maximum Junction Temperature must not be exceeded.
- The pins which are not defined may not be loaded by external signals.

## PIN CONNECTIONS



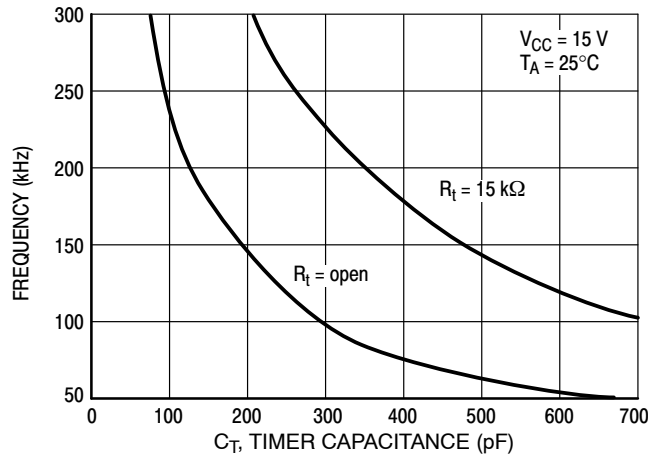
# NCP3163, NCV3163

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 15\text{ V}$ , Pin 16 =  $V_{CC}$ ,  $C_T = 270\text{ pF}$ ,  $R_T = 15\text{ k}\Omega$ , for typical values  $T_A = 25^\circ\text{C}$ , for min/max values  $T_A$  is the operating ambient temperature range that applies (Note 7), unless otherwise noted.)

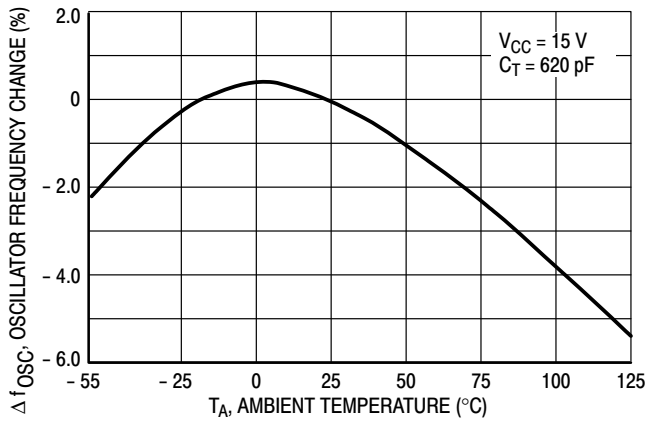
| Characteristic   | Symbol                             | Min              | Typ                      | Max                      | Unit          |
|--|------------------------------------|------------------|--------------------------|--------------------------|---------------|
| <b>OSCILLATOR</b>  |                                    |                  |                          |                          |               |
| Frequency<br>$T_A = 25^\circ\text{C}$ , $V_{CC} = 15\text{ V}$<br>Total Variation over $V_{CC} = 2.5\text{ V}$ to $40\text{ V}$ and Temperature  | $f_{\text{OSC}}$                   | 225<br>212       | 250<br>250               | 275<br>288               | kHz           |
| Charge Current   | $I_{\text{chg}}$                   | –                | 225                      | –                        | $\mu\text{A}$ |
| Discharge Current  | $I_{\text{dischg}}$                | –                | 25                       | –                        | $\mu\text{A}$ |
| Charge to Discharge Current Ratio  | $I_{\text{chg}}/I_{\text{dischg}}$ | 8.0<br>7.0       | 9.0<br>9.0               | 10.5<br>10.5             | –             |
| Sawtooth Peak Voltage  | $V_{\text{OSC(P)}}$                | –                | 1.25                     | –                        | V             |
| Sawtooth Valley Voltage  | $V_{\text{OSC(V)}}$                | –                | 0.55                     | –                        | V             |
| <b>FEEDBACK COMPARATOR 1</b>   |                                    |                  |                          |                          |               |
| Threshold Voltage<br>$T_A = 25^\circ\text{C}$<br>Total Variation over $V_{CC} = 2.5\text{ V}$ to $40\text{ V}$ and Temperature   | $V_{\text{th(FB1)}}$               | 4.9<br>4.85      | 5.05<br>–                | 5.2<br>5.25              | V             |
| Threshold Voltage – Line Regulation ( $V_{CC} = 2.5\text{ V}$ to $40\text{ V}$ , $T_A = 25^\circ\text{C}$ )  | $\text{REGline}_{(\text{FB1})}$    | –                | 0.008                    | 0.03                     | %/V           |
| Input Bias Current ( $V_{\text{FB1}} = 5.05\text{ V}$ )  | $I_{\text{B(FB1)}}$                | –                | 100                      | 200                      | $\mu\text{A}$ |
| <b>FEEDBACK COMPARATOR 2</b>   |                                    |                  |                          |                          |               |
| Threshold Voltage<br>$T_A = 25^\circ\text{C}$ , $V_{CC} = 15\text{ V}$<br>Total Variation over $V_{CC} = 2.5\text{ V}$ to $40\text{ V}$ and Temperature  | $V_{\text{th(FB2)}}$               | 1.225<br>1.213   | 1.25<br>–                | 1.275<br>1.287           | V             |
| Threshold Voltage – Line Regulation ( $V_{CC} = 2.5\text{ V}$ to $40\text{ V}$ , $T_A = 25^\circ\text{C}$ )  | $\text{REGline}_{(\text{FB1})}$    | –                | 0.008                    | 0.03                     | %/V           |
| Input Bias Current ( $V_{\text{FB2}} = 1.25\text{ V}$ )  | $I_{\text{B(FB2)}}$                | –0.4             | –                        | 0.4                      | $\mu\text{A}$ |
| <b>CURRENT LIMIT COMPARATOR</b>  |                                    |                  |                          |                          |               |
| Threshold Voltage<br>$T_A = 25^\circ\text{C}$<br>Total Variation over $V_{CC} = 2.5\text{ V}$ to $40\text{ V}$ , and Temperature   | $V_{\text{th(Sense)}}$             | –<br>225         | 250<br>–                 | –<br>270                 | mV            |
| Input Bias Current ( $V_{\text{Ipk (Sense)}} = 15\text{ V}$ )  | $I_{\text{B(Sense)}}$              | –                | 1.0                      | 20                       | $\mu\text{A}$ |
| <b>DRIVER AND OUTPUT SWITCH (Note 6)</b>   |                                    |                  |                          |                          |               |
| Saturation Voltage ( $I_{\text{SW}} = 2.5\text{ A}$ , Pins 14, 15 grounded)<br>Non-Darlington ( $R_{\text{Pin 9}} = 110\ \Omega$ to $V_{CC}$ , $I_{\text{SW}}/I_{\text{DRV}} \approx 20$ )<br>Darlington Connection (Pins 9, 10, 11 connected) | $V_{\text{CE(sat)}}$               | –<br>–<br>–<br>– | 0.6<br>0.6<br>1.0<br>1.0 | 1.0<br>1.5<br>1.4<br>1.5 | V             |
| Collector Off-State Leakage Current ( $V_{\text{CE}} = 40\text{ V}$ )  | $I_{\text{C(off)}}$                | –                | 0.02                     | 100                      | $\mu\text{A}$ |
| Bootstrap Input Current Source ( $V_{\text{BS}} = V_{CC} + 5.0\text{ V}$ )   | $I_{\text{source(DRV)}}$           | 0.5              | 2.0                      | 4.0                      | mA            |
| Bootstrap Input Zener Clamp Voltage ( $I_{\text{Z}} = 25\text{ mA}$ )  | $V_{\text{Z}}$                     | $V_{CC} + 6.0$   | $V_{CC} + 7.0$           | $V_{CC} + 9.0$           | V             |
| <b>LOW VOLTAGE INDICATOR</b>   |                                    |                  |                          |                          |               |
| Input Threshold ( $V_{\text{FB2}}$ Increasing)   | $V_{\text{th}}$                    | 1.07             | 1.125                    | 1.18                     | V             |
| Input Hysteresis ( $V_{\text{FB2}}$ Decreasing)  | $V_{\text{H}}$                     | –                | 15                       | –                        | mV            |
| Output Sink Saturation Voltage ( $I_{\text{sink}} = 2.0\text{ mA}$ )   | $V_{\text{OL(LVI)}}$               | –                | 0.15                     | 0.4                      | V             |
| Output Off-State Leakage Current ( $V_{\text{OH}} = 15\text{ V}$ )   | $I_{\text{OH}}$                    | –                | 0.01                     | 5.0                      | $\mu\text{A}$ |
| <b>TOTAL DEVICE</b>  |                                    |                  |                          |                          |               |
| Standby Supply Current ( $V_{CC} = 2.5\text{ V}$ to $40\text{ V}$ , Pin 8 = $V_{CC}$ , Pins 6, 14, 15 = GND, remaining pins open)  | $I_{\text{CC}}$                    | –                | 6.0                      | 10                       | mA            |

5. Maximum package power dissipation limits must be observed.
6. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
7.  $T_{\text{low}} = 0^\circ\text{C}$  for NCP3163       $T_{\text{high}} = +70^\circ\text{C}$  for NCP3163  
     =  $-40^\circ\text{C}$  for NCP3163B      =  $+85^\circ\text{C}$  for NCP3163B  
     =  $-40^\circ\text{C}$  for NCV3163      =  $+125^\circ\text{C}$  for NCV3163

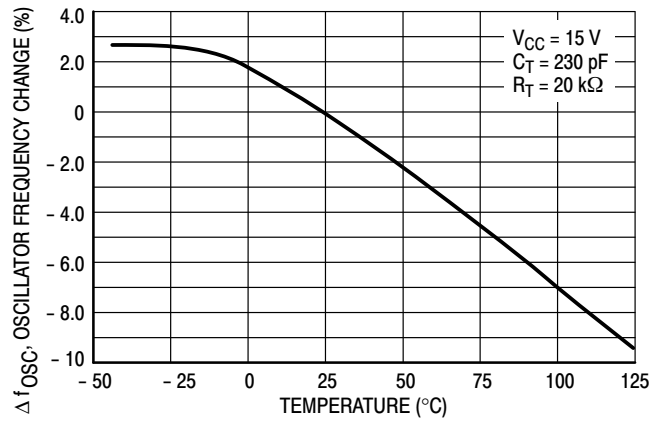
# NCP3163, NCV3163



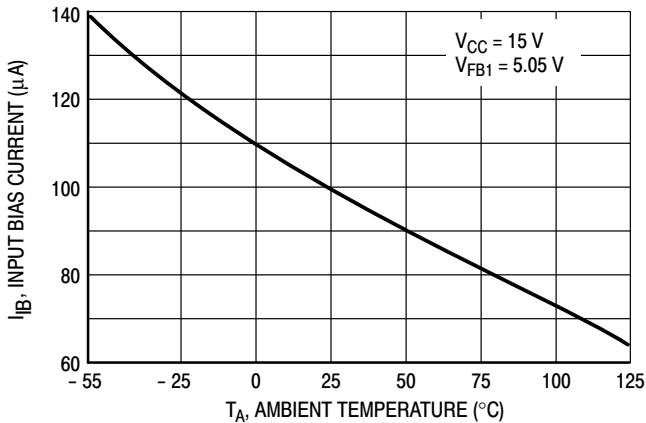
**Figure 3. Oscillator Frequency vs. Timer Capacitance ( $C_T$ )**



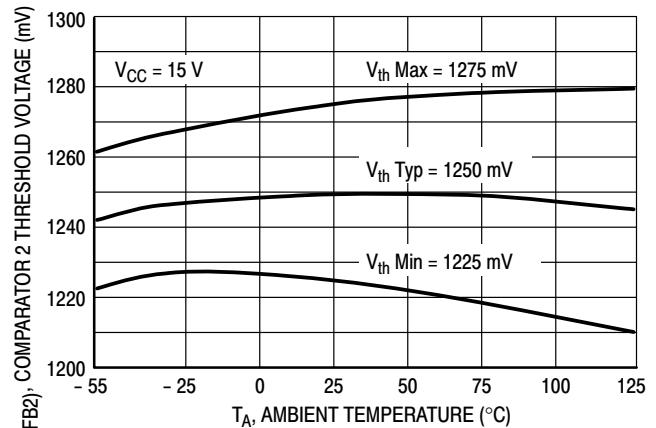
**Figure 4. Oscillator Frequency Change vs. Temperature when only  $C_T$  is connected to Pin 6**



**Figure 5. Oscillator Frequency Change vs. Temperature when  $C_T$  and  $R_T$  are connected to Pin 6**

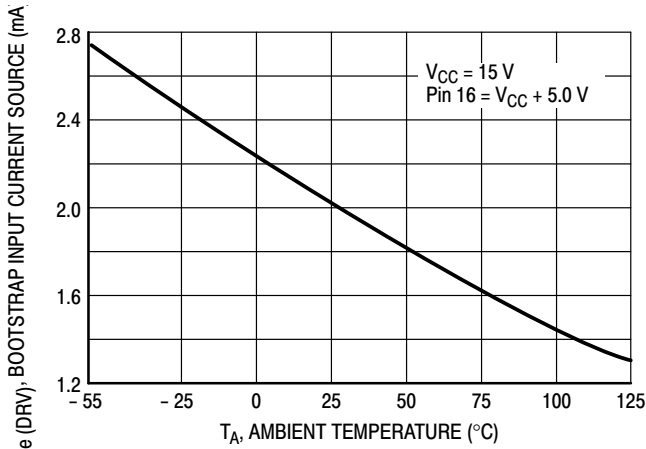


**Figure 6. Feedback Comparator 1 Input Bias Current vs. Temperature**

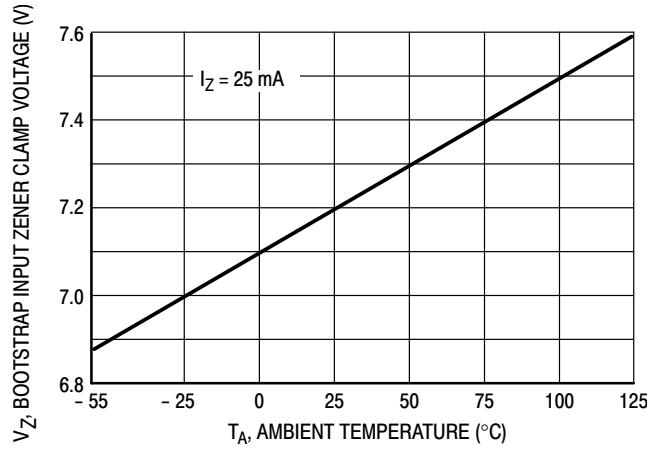


**Figure 7. Feedback Comparator 2 Threshold Voltage vs. Temperature**

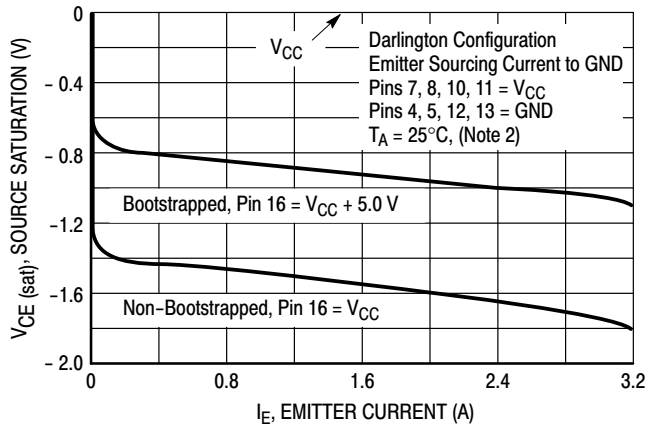
# NCP3163, NCV3163



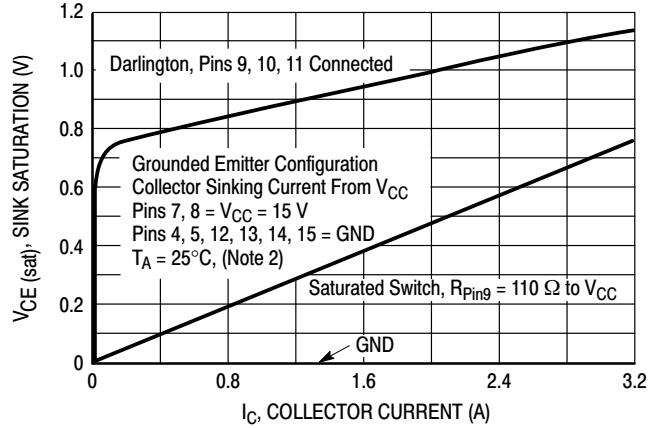
**Figure 8. Bootstrap Input Current Source vs. Temperature**



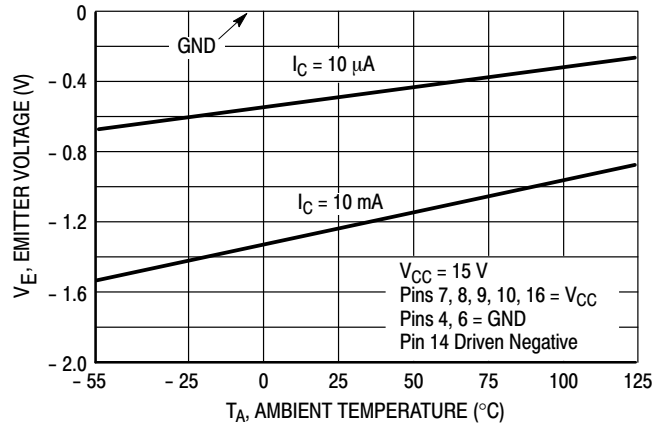
**Figure 9. Bootstrap Input Zener Clamp Voltage vs. Temperature**



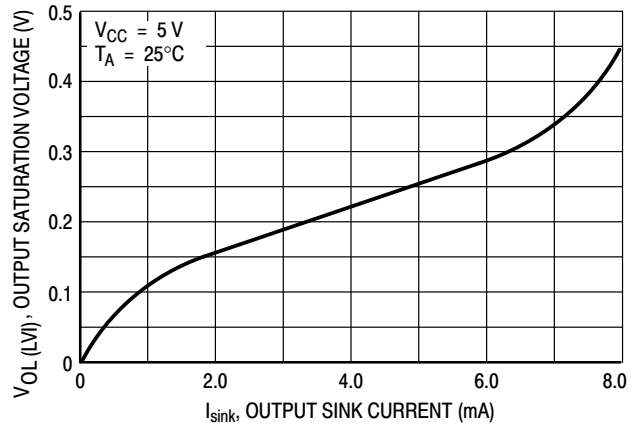
**Figure 10. Output Switch Source Saturation vs. Emitter Current**



**Figure 11. Output Switch Sink Saturation vs. Collector Current**

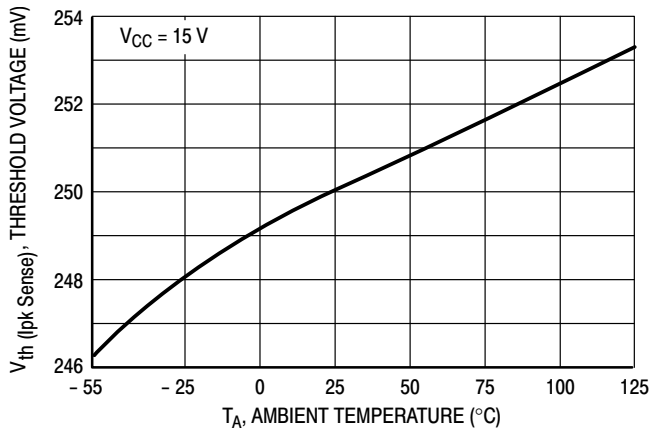


**Figure 12. Output Switch Negative Emitter Voltage vs. Temperature**

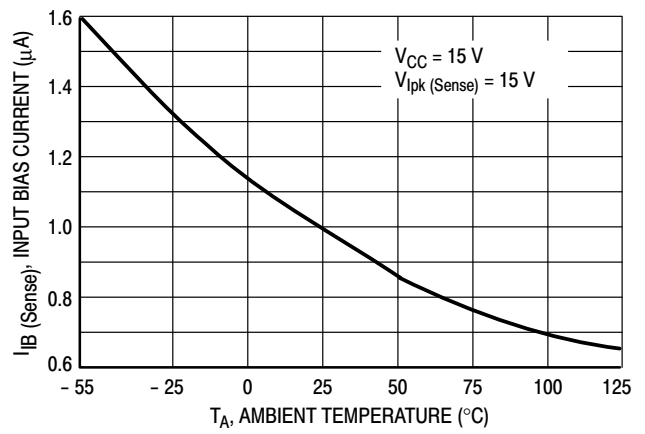


**Figure 13. Low Voltage Indicator Output Sink Saturation Voltage vs. Sink Current**

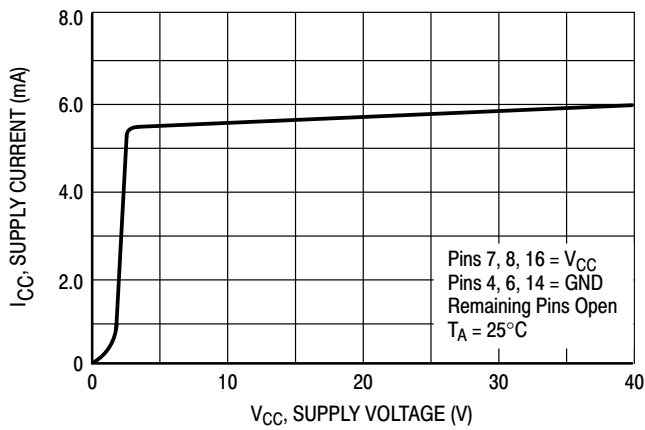
# NCP3163, NCV3163



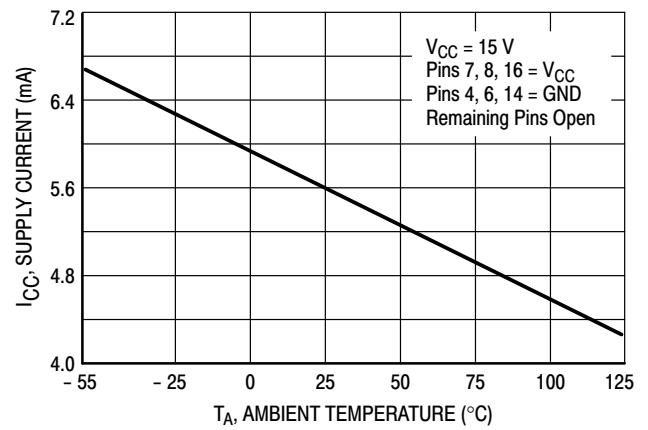
**Figure 14. Current Limit Comparator Threshold Voltage vs. Temperature**



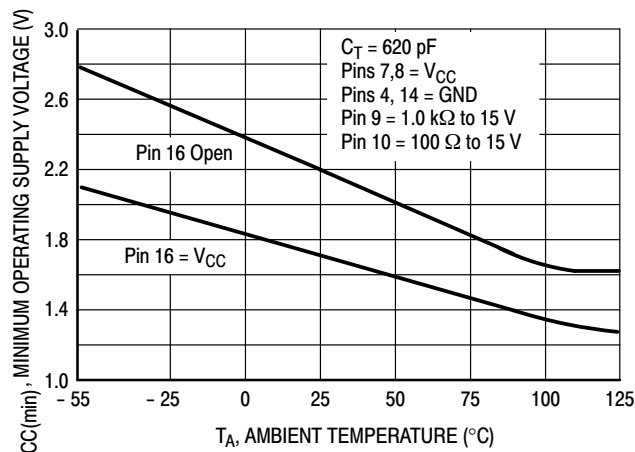
**Figure 15. Current Limit Comparator Input Bias Current vs. Temperature**



**Figure 16. Standby Supply Current vs. Supply Voltage**



**Figure 17. Standby Supply Current vs. Temperature**



**Figure 18. Minimum Operating Supply Voltage vs. Temperature**

INTRODUCTION

The NCP3163 is a monolithic power switching regulator optimized for DC-to-DC converter applications. The combination of its features enables the system designer to directly implement step-up, step-down, and voltage-inverting converters with a minimum number of external components. Potential applications include cost sensitive consumer products as well as equipment for the automotive, computer, and industrial markets. A representative block diagram is shown in Figure 2.

OPERATING DESCRIPTION

The NCP3163 operates as a fixed on-time, variable off-time voltage mode ripple regulator. In general, this mode of operation is somewhat analogous to a capacitor charge pump and does not require dominant pole loop compensation for converter stability. The Typical Operating Waveforms are shown in Figure 19. The output voltage waveform shown is for a step-down converter with the ripple and phasing exaggerated for clarity. During initial converter startup, the feedback comparator senses that the output voltage level is below nominal. This causes the output switch to turn on and off at a frequency and duty cycle controlled by the oscillator, thus pumping up the output filter capacitor. When the output voltage level reaches nominal, the feedback comparator sets the latch, immediately terminating switch conduction. The feedback comparator will inhibit the switch until the load current causes the output voltage to fall below nominal. Under these conditions, output switch conduction can be inhibited for a partial

oscillator cycle, a partial cycle plus a complete cycle, multiple cycles, or a partial cycle plus multiple cycles.

Oscillator

The oscillator frequency and on-time of the output switch are programmed by the value selected for timing capacitor  $C_T$ . Capacitor  $C_T$  is charged and discharged by a 9 to 1 ratio internal current source and sink, generating a negative going sawtooth waveform at Pin 6. As  $C_T$  charges, an internal pulse is generated at the oscillator output. This pulse is connected to the NOR gate center input, preventing output switch conduction, and to the AND gate upper input, allowing the latch to be reset if the comparator output is low. Thus, the output switch is always disabled during ramp-up and can be enabled by the comparator output only at the start of ramp-down. The oscillator peak and valley thresholds are 1.25 V and 0.55 V, respectively, with a charge current of 225  $\mu$ A and a discharge current of 25  $\mu$ A, yielding a maximum on-time duty cycle of 90%. A reduction of the maximum duty cycle may be required for specific converter configurations. This can be accomplished with the addition of an external deadtime resistor ( $R_{DT}$ ) placed across  $C_T$ . The resistor increases the discharge current which reduces the on-time of the output switch. The converter output can be inhibited by clamping  $C_T$  to ground with an external NPN small-signal transistor. To calculate the frequency when only  $C_T$  is connected to Pin 6, use the equations found in Figure 22. When  $R_T$  is also used, the frequency and maximum duty cycle can be calculated with the NCP3163 design tool found at [www.onsemi.com](http://www.onsemi.com).

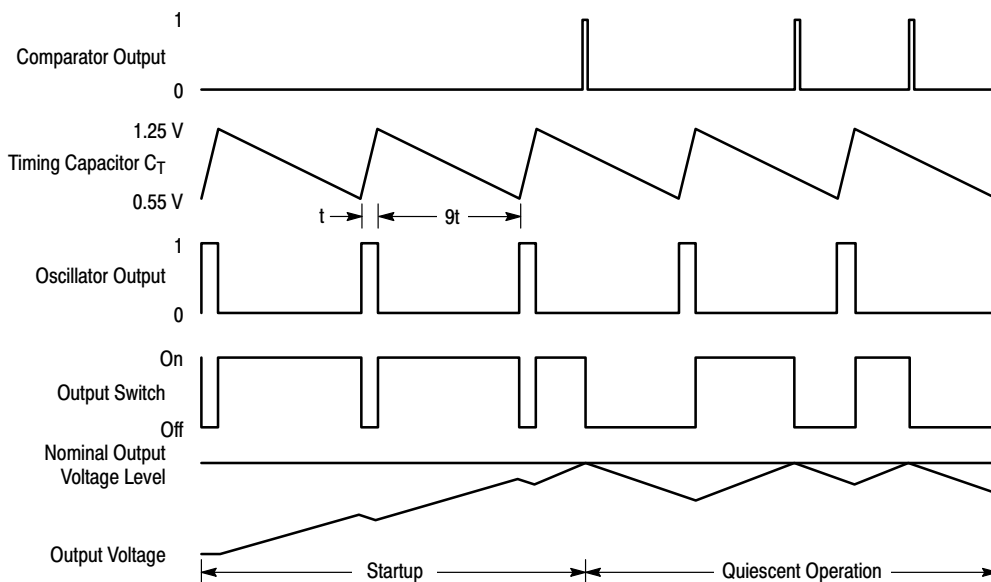


Figure 19. Typical Operating Waveforms



### Feedback and Low Voltage Indicator Comparators

Output voltage control is established by the Feedback comparator. The inverting input is internally biased at 1.25 V and is not pinned out. The converter output voltage is typically divided down with two external resistors and monitored by the high impedance noninverting input at Pin 2. The maximum input bias current is  $\pm 0.4 \mu\text{A}$ , which can cause an output voltage error that is equal to the product of the input bias current and the upper divider resistance value. For applications that require 5.0 V, the converter output can be directly connected to the noninverting input at Pin 3. The high impedance input, Pin 2, must be grounded to prevent noise pickup. The internal resistor divider is set for a nominal voltage of 5.05 V. The additional 50 mV compensates for a 1.0% voltage drop in the cable and connector from the converter output to the load. The Feedback comparator's

output state is controlled by the highest voltage applied to either of the two noninverting inputs.

The Low Voltage Indicator (LVI) comparator is designed for use as a reset controller in microprocessor-based systems. The inverting input is internally biased at 1.125 V, which sets the noninverting input thresholds to 90% of nominal. The LVI comparator has 15 mV of hysteresis to prevent erratic reset operation. The Open Collector output is capable of sinking in excess of 6.0 mA (see Figure 13). An external resistor ( $R_{LVI}$ ) and capacitor ( $C_{DLY}$ ) can be used to program a reset delay time ( $t_{DLY}$ ) by the formula shown below, where  $V_{th(MPU)}$  is the microprocessor reset input threshold. Refer to Figure 20.

$$t_{DLY} = R_{LVI} \cdot C_{DLY} \cdot \ln \left( \frac{1}{1 - \frac{V_{th(MPU)}}{V_{out}}} \right)$$

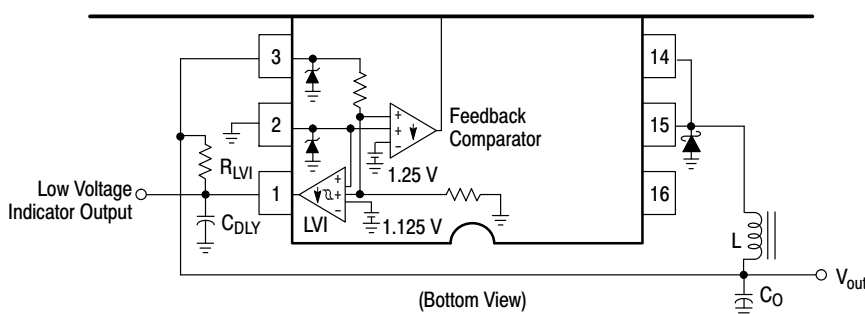


Figure 20. Partial Application Schematic Showing Implementation of LVI Delay with  $R_{LVI}$  and  $C_{DLY}$

### Current Limit Comparator, Latch and Thermal Shutdown

With a voltage mode ripple converter operating under normal conditions, output switch conduction is initiated by the oscillator and terminated by the Voltage Feedback comparator. Abnormal operating conditions occur when the converter output is overloaded or when feedback voltage sensing is lost. Under these conditions, the Current Limit comparator will protect the Output Switch.

The switch current is converted to a voltage by inserting a fractional ohm resistor,  $R_{SC}$ , in series with  $V_{CC}$  and output switch transistor  $Q_2$ . The voltage drop across  $R_{SC}$  is monitored by the Current Sense comparator. If the voltage drop exceeds 250 mV with respect to  $V_{CC}$ , the comparator will set the latch and terminate output switch conduction on a cycle-by-cycle basis. This Comparator/Latch configuration ensures that the Output Switch has only a single on-time during a given oscillator cycle. The calculation for a value of  $R_{SC}$  is:

$$R_{SC} = \frac{0.25 \text{ V}}{I_{pk} \text{ (Switch)}}$$

Figures 14 and 15 show that the Current Sense comparator threshold is tightly controlled over temperature and has a typical input bias current of  $1.0 \mu\text{A}$ . The propagation delay from the comparator input to the Output Switch is typically

200 ns. The parasitic inductance associated with  $R_{SC}$  and the circuit layout should be minimized. This will prevent unwanted voltage spikes that may falsely trip the Current Limit comparator.

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. When activated, typically at  $170^\circ\text{C}$ , the Latch is forced into the "Set" state, disabling the Output Switch. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a replacement for proper heatsinking.

### Driver and Output Switch

To aid in system design flexibility and conversion efficiency, the driver current source and collector, and output switch collector and emitter are pinned out separately. This allows the designer the option of driving the output switch into saturation with a selected force gain or driving it near saturation when connected as a Darlington. The output switch has a typical current gain of 70 at 2.5 A and is designed to switch a maximum of 40 V collector to emitter, with up to 3.4 A peak collector current. The minimum value for  $R_{SC}$  is:

$$R_{SC(\text{min})} = \frac{0.25 \text{ V}}{3.4 \text{ A}} = 0.0735 \Omega$$

## NCP3163, NCV3163

When configured for step-down or voltage-inverting applications (see application notes at the end of this document) the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn-on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency.

Figure 12 shows that by clamping the emitter to 0.5 V, the collector current will be in the range 10  $\mu$ A over temperature. A 1N5822 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

A bootstrap input is provided to reduce the output switch saturation voltage in step-down and voltage-inverting converter applications. This input is connected through a series resistor and capacitor to the switch emitter and is used to raise the internal 2.0 mA bias current source above  $V_{CC}$ . An internal zener limits the bootstrap input voltage to  $V_{CC} + 7.0$  V. The capacitor's equivalent series resistance must limit the zener current to less than 100 mA. An additional series resistor may be required when using tantalum or other

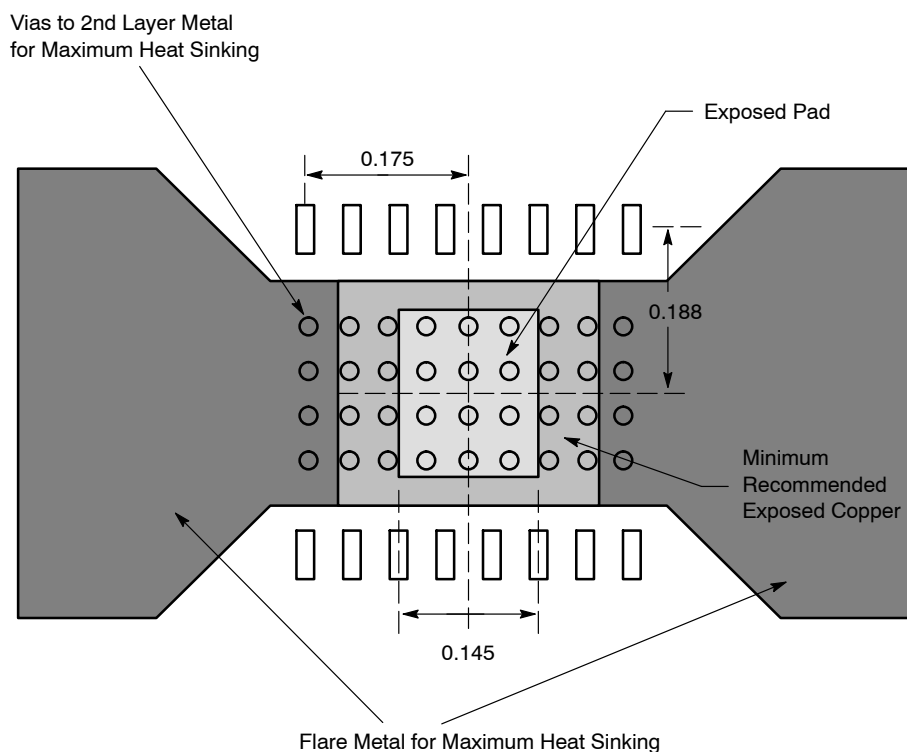
low ESR capacitors. The equation below is used to calculate a minimum value bootstrap capacitor based on a minimum zener voltage and an upper limit current source.

$$C_{B(\min)} = I \frac{\Delta t}{\Delta V} = 4.0 \text{ mA} \frac{t_{\text{on}}}{4.0 \text{ V}} = 0.001 t_{\text{on}}$$

Parametric operation of the NCP3163 is guaranteed over a supply voltage range of 2.5 V to 40 V. When operating below 3.0 V, the Bootstrap Input should be connected to  $V_{CC}$ . Figure 18 shows that functional operation down to 1.7 V at room temperature is possible.

### Package

The NCP3163 is contained in a heatsinkable 16-lead plastic package in which the die is mounted on a special heat tab copper alloy pad. This pad is designed to be soldered directly to a GND connection on the printed circuit board to improve thermal conduction. Since this pad directly contacts the substrate of the die, it is important that this pad be always soldered to GND, even if surface mount heat sinking is not being used. Figure 21 shows recommended layout techniques for this package.



**Figure 21. Layout Guidelines to Obtain Maximum Package Power Dissipation**

## APPLICATIONS

Figures 23 through 30 show the simplicity and flexibility of the NCP3163. Three main converter topologies are demonstrated with actual test data shown below each of the circuit diagrams. Figure 22 gives the relevant design

equations for the key parameters. Additionally, a complete application design aid for the NCP3163 can be found at [www.onsemi.com](http://www.onsemi.com).

## NCP3163, NCV3163

| Calculation                                   | Step-Down  | Step-Up  | Voltage-Inverting  |
|---|--|--|--|
| (See Notes 1,2,3)<br>$\frac{t_{on}}{t_{off}}$ | $\frac{V_{out} + V_F}{V_{in} - V_{sat} - V_{out}}$                           | $\frac{V_{out} + V_F \frac{V_{in}}{V_{sat}}}{V_{in} \frac{V_{in}}{V_{sat}}}$ | $\frac{ V_{out}  + V_F}{V_{in} - V_{sat}}$                                   |
| $t_{on}$                                      | $\frac{\frac{t_{on}}{t_{off}}}{f \left( \frac{t_{on}}{t_{off}} + 1 \right)}$ | $\frac{\frac{t_{on}}{t_{off}}}{f \left( \frac{t_{on}}{t_{off}} + 1 \right)}$ | $\frac{\frac{t_{on}}{t_{off}}}{f \left( \frac{t_{on}}{t_{off}} + 1 \right)}$ |
| $C_T$   | $\frac{32.143 \cdot 10^{-6}}{f} - 20 \cdot 10^{-12}$                         | $\frac{32.143 \cdot 10^{-6}}{f} - 20 \cdot 10^{-12}$                         | $\frac{32.143 \cdot 10^{-6}}{f} - 20 \cdot 10^{-12}$                         |
| $I_{L(av)}$                                   | $I_{out}$  | $I_{out} \left( \frac{t_{on}}{t_{off}} + 1 \right)$                          | $I_{out} \left( \frac{t_{on}}{t_{off}} + 1 \right)$                          |
| $I_{pk} \text{ (Switch)}$                     | $I_{L(av)} + \frac{\Delta I_L}{2}$   | $I_{L(av)} + \frac{\Delta I_L}{2}$   | $I_{L(av)} + \frac{\Delta I_L}{2}$   |
| $R_{SC}$                                      | $\frac{0.25}{I_{pk} \text{ (Switch)}}$                                       | $\frac{0.25}{I_{pk} \text{ (Switch)}}$                                       | $\frac{0.25}{I_{pk} \text{ (Switch)}}$                                       |
| $L$   | $\left( \frac{V_{in} - V_{sat} - V_{out}}{\Delta I_L} \right) t_{on}$        | $\left( \frac{V_{in} - V_{sat}}{\Delta I_L} \right) t_{on}$                  | $\left( \frac{V_{in} - V_{sat}}{\Delta I_L} \right) t_{on}$                  |
| $V_{ripple(pp)}$                              | $\Delta I_L \sqrt{\left( \frac{1}{8 f C_O} \right)^2 + (ESR)^2}$             | $\approx \frac{t_{on} I_{out}}{C_O}$   | $\approx \frac{t_{on} I_{out}}{C_O}$   |
| $V_{out}$                                     | $V_{ref} \left( \frac{R_2}{R_1} + 1 \right)$                                 | $V_{ref} \left( \frac{R_2}{R_1} + 1 \right)$                                 | $V_{ref} \left( \frac{R_2}{R_1} + 1 \right)$                                 |

**The following Converter Characteristics must be chosen:**

- $V_{in}$  – Nominal operating input voltage.
- $V_{out}$  – Desired output voltage.
- $I_{out}$  – Desired output current.
- $\Delta I_L$  – Desired peak-to-peak inductor ripple current. For maximum output current it is suggested that  $\Delta I_L$  be chosen to be less than 10% of the average inductor current  $I_{L(av)}$ . This will help prevent  $I_{pk} \text{ (Switch)}$  from reaching the current limit threshold set by  $R_{SC}$ . If the design goal is to use a minimum inductance value, let  $\Delta I_L = 2(I_{L(av)})$ . This will proportionally reduce converter output current capability.
- $f$  – Maximum output switch frequency.
- $V_{ripple(pp)}$  – Desired peak-to-peak output ripple voltage. For best performance the ripple voltage should be kept to a low value since it will directly affect line and load regulation. Capacitor  $C_O$  should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

- NOTES:**
1.  $V_{sat}$  – Saturation voltage of the output switch, refer to Figures 10 and 11.
  2.  $V_F$  – Output rectifier forward voltage drop. Typical value for 1N5822 Schottky barrier rectifier is 0.5 V.
  3. The calculated  $t_{on}/t_{off}$  must not exceed the minimum guaranteed oscillator charge to discharge ratio of 8, at the minimum operating input voltage.

**Figure 22. Design Equations**

# NCP3163, NCV3163

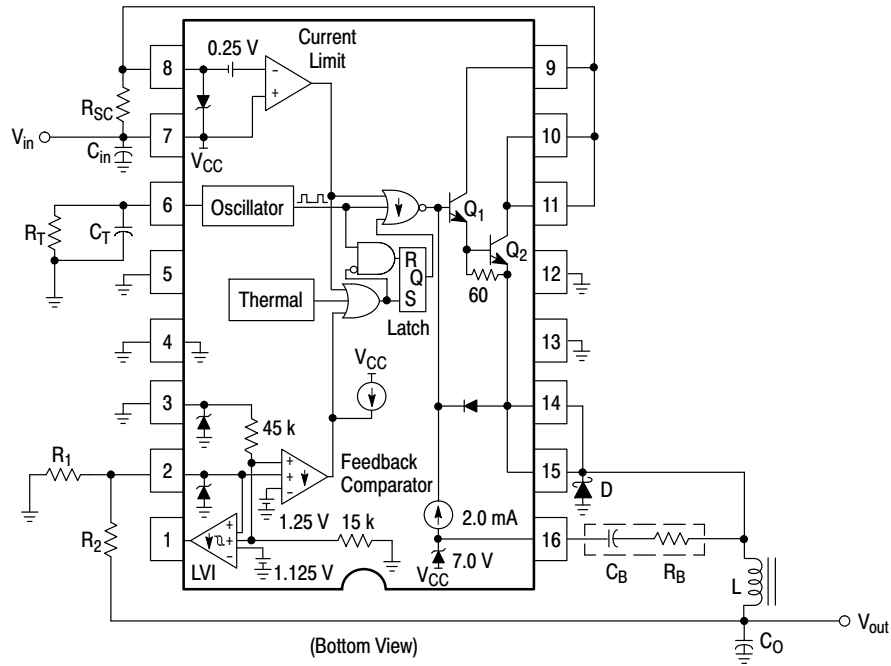


Figure 23. Typical Buck Application Schematic

### Value of Components

| Name             | Value                        |
|------------------|------------------------------|
| L                | 47 $\mu$ H                   |
| D                | 2 A, 40 V Schottky Rectifier |
| C <sub>in</sub>  | 47 $\mu$ F, 35 V             |
| C <sub>out</sub> | 100 $\mu$ F, 10 V            |
| C <sub>t</sub>   | 270 pF $\pm$ 10%             |
| R <sub>t</sub>   | 15 k $\Omega$                |

| Name            | Value               |
|-----------------|---------------------|
| R <sub>1</sub>  | 15 k $\Omega$       |
| R <sub>2</sub>  | 24.9 k $\Omega$     |
| R <sub>sc</sub> | 80 m $\Omega$ , 1 W |
| C <sub>b</sub>  | 4.7 nF              |
| R <sub>b</sub>  | 200 $\Omega$        |

### Test Results for V<sub>out</sub> = 3.3 V

| Test                  | Condition   | Results  |
|-----------------------|---|----------|
| Line Regulation       | V <sub>in</sub> = 8.0 V to 24 V, I <sub>out</sub> = 2.5 A | 13 mV    |
| Load Regulation       | V <sub>in</sub> = 12 V, I <sub>out</sub> = 0 to 2.5 A     | 25 mV    |
| Output Ripple         | V <sub>in</sub> = 12 V, I <sub>out</sub> = 0 to 2.5 A     | 100 mVpp |
| Efficiency            | V <sub>in</sub> = 12 V, I <sub>out</sub> = 2.5 A          | 70.3%    |
| Short Circuit Current | V <sub>in</sub> = 12 V, R <sub>L</sub> = 0.1 $\Omega$     | 3.1 A    |

### Test Results for V<sub>out</sub> = 5.05 V

| Test                  | Condition  | Results  |
|-----------------------|--|----------|
| Line Regulation       | V <sub>in</sub> = 10.2 V to 24 V, I <sub>out</sub> = 2.5 A | 54 mV    |
| Load Regulation       | V <sub>in</sub> = 12 V, I <sub>out</sub> = 0 to 2.5 A      | 28 mV    |
| Output Ripple         | V <sub>in</sub> = 12 V, I <sub>out</sub> = 0 to 2.5 A      | 150 mVpp |
| Efficiency            | V <sub>in</sub> = 12 V, I <sub>out</sub> = 2.5 A           | 75.5%    |
| Short Circuit Current | V <sub>in</sub> = 12 V, R <sub>L</sub> = 0.1 $\Omega$      | 3.1 A    |

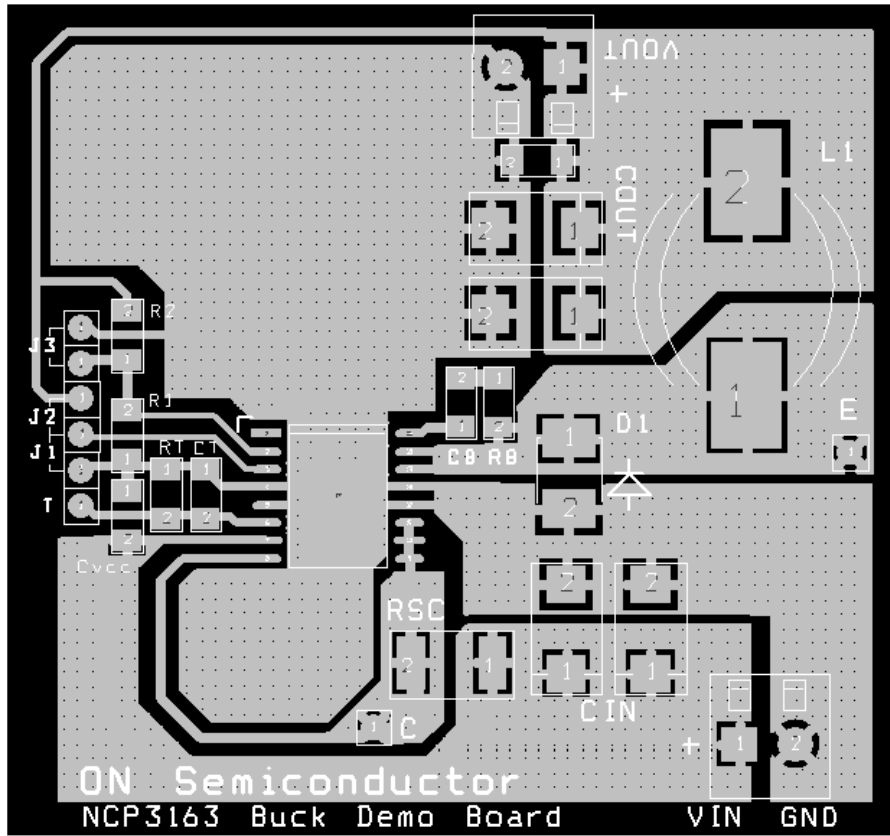


Figure 24. Buck Layout

APPLICATION SPECIFIC CHARACTERISTICS

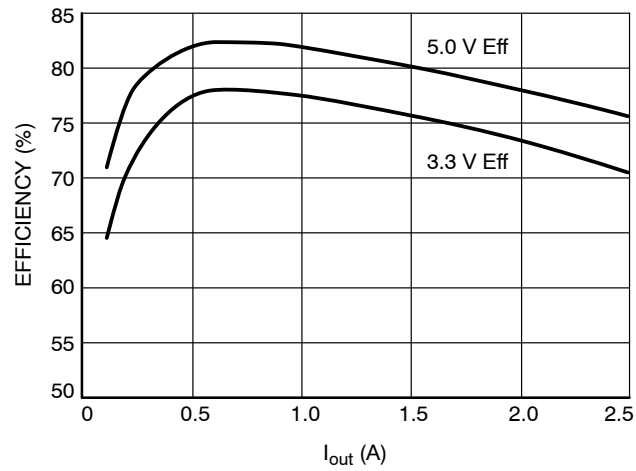


Figure 25. Efficiency vs. Output Current for the Buck Demo Board at  $V_{in} = 12\text{ V}$ ,  $T_A = 25^\circ\text{C}$

# NCP3163, NCV3163

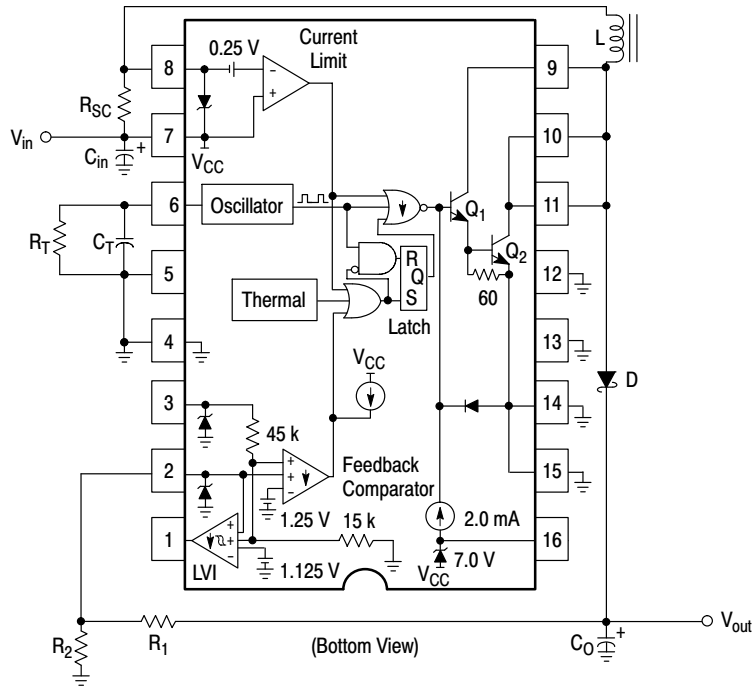


Figure 26. Typical Boost Application Schematic

### Value of Components for $V_{out} = 24\text{ V}$

| Name     | Value                        |
|----------|------------------------------|
| L        | 33 $\mu\text{H}$             |
| D        | 2 A, 40 V Schottky Rectifier |
| $C_{in}$ | 330 $\mu\text{F}$ , 35 V     |
| $C_t$    | 270 pF $\pm 10\%$            |
| $R_t$    | 15 k $\Omega$                |

| Name      | Value                    |
|-----------|--------------------------|
| $R_1$     | 42.2 k $\Omega$          |
| $R_2$     | 2.32 k $\Omega$          |
| $C_{out}$ | 330 $\mu\text{F}$ , 25 V |
| $R_{sc}$  | 80 m $\Omega$ , 1 W      |

### Test Results for $V_{out} = 24\text{ V}$

| Test                  | Condition  | Results  |
|-----------------------|--|----------|
| Line Regulation       | $V_{in} = 10\text{ V to } 20\text{ V}$ , $I_{out} = 700\text{ mA}$ | 90 mV    |
| Load Regulation       | $V_{in} = 12\text{ V}$ , $I_{out} = 0\text{ to } 700\text{ mA}$    | 80 mV    |
| Output Ripple         | $V_{in} = 12\text{ V}$ , $I_{out} = 0\text{ to } 700\text{ mA}$    | 300 mVpp |
| Efficiency            | $V_{in} = 12\text{ V}$ , $I_{out} = 700\text{ mA}$                 | 83%      |
| Short Circuit Current | $V_{in} = 12\text{ V}$ , $R_L = 0.1\ \Omega$                       | 3.1 A    |

# NCP3163, NCV3163

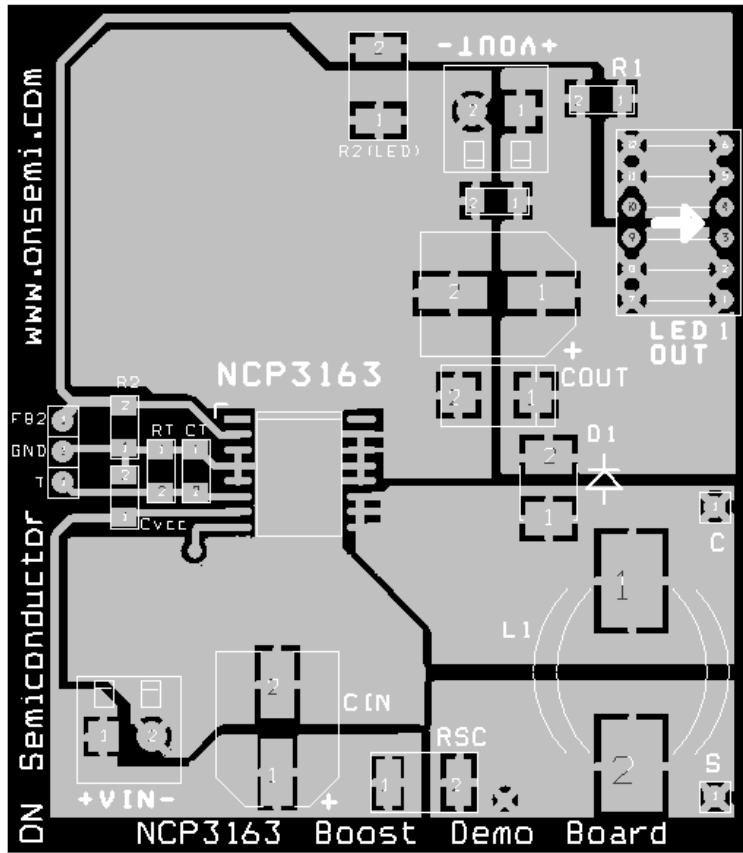


Figure 27. Boost Demo Board Layout

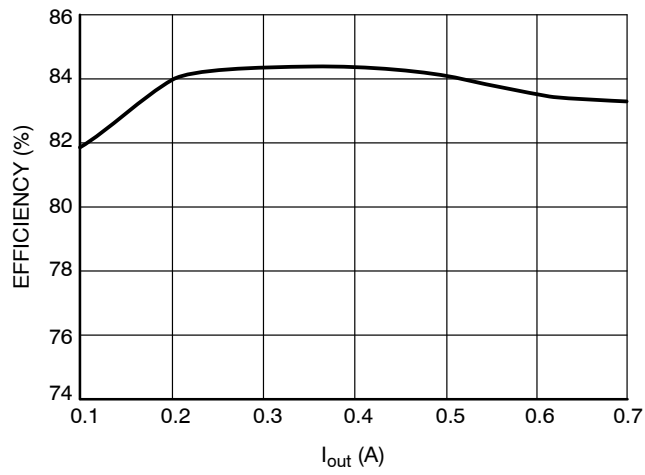
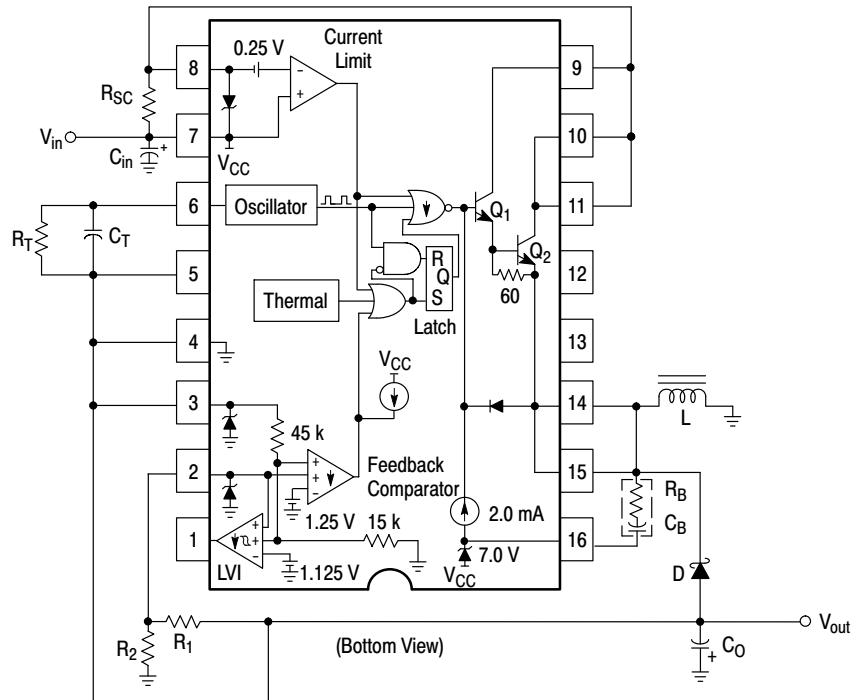


Figure 28. Efficiency vs. Output Current for the Boost Demo Board at  $V_{in} = 12\text{ V}$ ,  $T_A = 25^\circ\text{C}$

## NCP3163, NCV3163



**Figure 29. Typical Voltage Inverting Application Schematic**

### Value of Components for $V_{out} = -15\text{ V}$

| Name      | Value                        |
|-----------|------------------------------|
| L         | 47 $\mu\text{H}$             |
| D         | 2 A, 40 V Schottky Rectifier |
| $C_{in}$  | 270 $\mu\text{F}$ , 16 V     |
| $C_{out}$ | 2 X 270 $\mu\text{F}$ , 16 V |
| $C_t$     | 150 pF $\pm 10\%$            |

| Name     | Value               |
|----------|---------------------|
| $R_1$    | 1.07 k $\Omega$     |
| $R_2$    | 11.8 k $\Omega$     |
| $R_{sc}$ | 80 m $\Omega$ , 1 W |
| $C_b$    | 4.7 nF              |
| $R_b$    | 200 m $\Omega$      |

### Test Results for $V_{out} = -15\text{ V}$

| Test                  | Condition  | Results  |
|-----------------------|--|----------|
| Line Regulation       | $V_{in} = 7.0\text{ V to }16\text{ V}$ , $I_{out} = 500\text{ mA}$ | 35 mV    |
| Load Regulation       | $V_{in} = 12\text{ V}$ , $I_{out} = 0\text{ to }500\text{ mA}$     | 20 mV    |
| Output Ripple         | $V_{in} = 12\text{ V}$ , $I_{out} = 0\text{ to }500\text{ mA}$     | 100 mVpp |
| Efficiency            | $V_{in} = 12\text{ V}$ , $I_{out} = 500\text{ mA}$                 | 68%      |
| Short Circuit Current | $V_{in} = 12\text{ V}$ , $R_L = 0.1\ \Omega$                       | 3.1 A    |



NCP3163, NCV3163

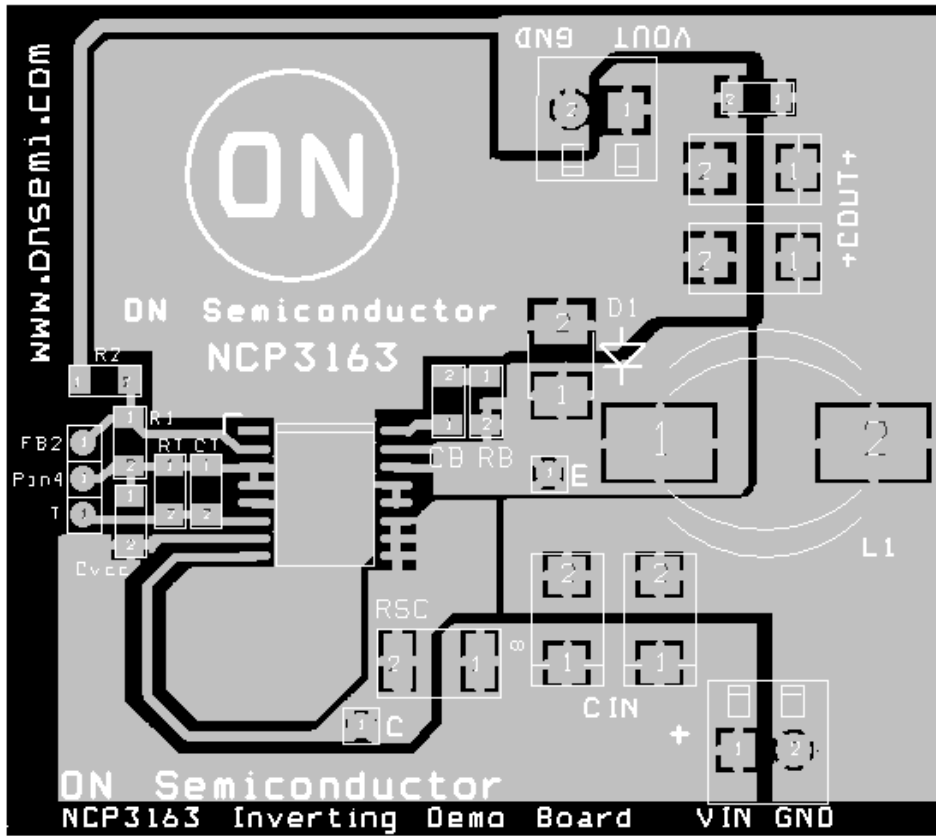


Figure 30. Voltage Inverting Demo Board Layout

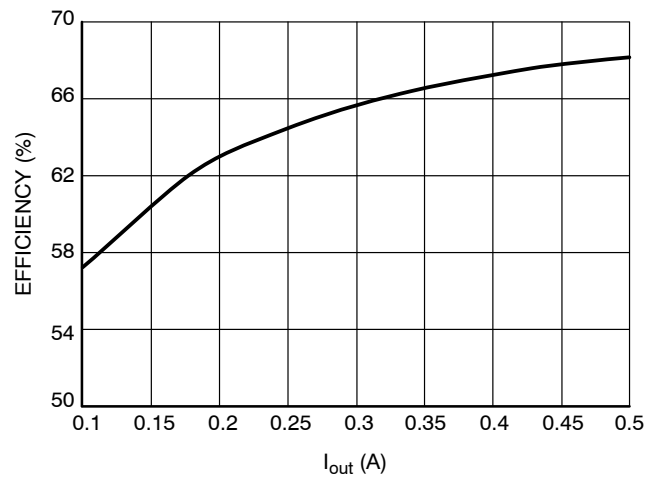


Figure 31. Efficiency vs. Output Current for the Voltage Inverting Demo Board at  $V_{in} = 12$  V,  $T_A = 25^\circ\text{C}$

## NCP3163, NCV3163

### ORDERING INFORMATION

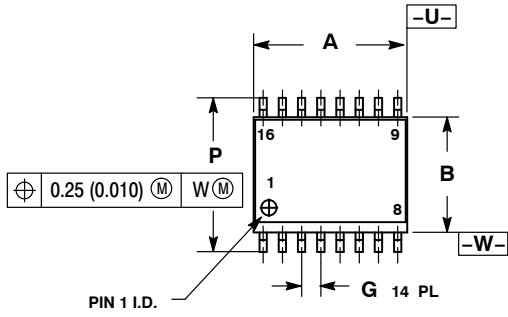
| Device        | Package                            | Shipping†          |
|---------------|------------------------------------|--------------------|
| NCP3163PWG    | SOIC-16 W Exposed Pad<br>(Pb-Free) | 47 Units / Rail    |
| NCP3163PWR2G  | SOIC-16 W Exposed Pad<br>(Pb-Free) | 1000 / Tape & Reel |
| NCP3163BPWG   | SOIC-16 W Exposed Pad<br>(Pb-Free) | 47 Units / Rail    |
| NCP3163BPWR2G | SOIC-16 W Exposed Pad<br>(Pb-Free) | 1000 / Tape & Reel |
| NCP3163MNR2G  | DFN18<br>(Pb-Free)                 | 2500 / Tape & Reel |
| NCP3163BMNR2G | DFN18<br>(Pb-Free)                 | 2500 / Tape & Reel |
| NCV3163PWG    | SOIC-16 W Exposed Pad<br>(Pb-Free) | 47 Units / Rail    |
| NCV3163PWR2G  | SOIC-16 W Exposed Pad<br>(Pb-Free) | 1000 / Tape & Reel |
| NCV3163MNR2G  | DFN18<br>(Pb-Free)                 | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

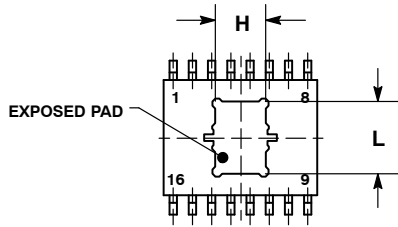
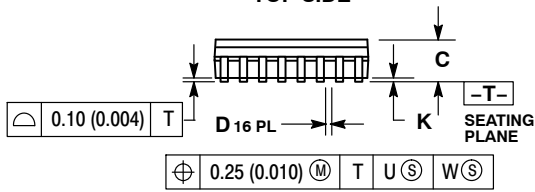
# NCP3163, NCV3163

## PACKAGE DIMENSIONS

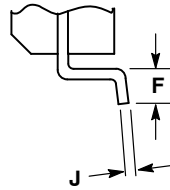
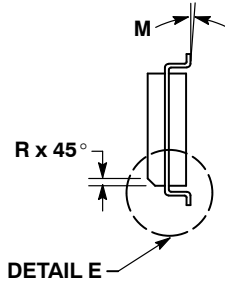
SOIC 16 LEAD WIDE BODY, EXPOSED PAD  
PW SUFFIX  
CASE 751AG-01  
ISSUE A



TOP SIDE



BACK SIDE

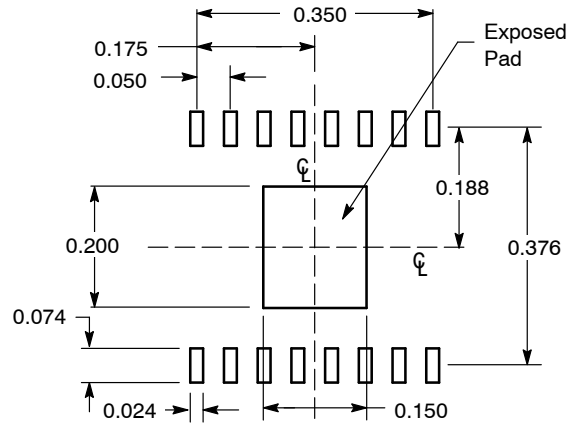


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751R-01 OBSOLETE, NEW STANDARD 751R-02.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 10.15       | 10.45 | 0.400     | 0.411 |
| B   | 7.40        | 7.60  | 0.292     | 0.299 |
| C   | 2.35        | 2.65  | 0.093     | 0.104 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.50        | 0.90  | 0.020     | 0.035 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| H   | 3.45        | 3.66  | 0.136     | 0.144 |
| J   | 0.25        | 0.32  | 0.010     | 0.012 |
| K   | 0.00        | 0.10  | 0.000     | 0.004 |
| L   | 4.72        | 4.93  | 0.186     | 0.194 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 10.05       | 10.55 | 0.395     | 0.415 |
| R   | 0.25        | 0.75  | 0.010     | 0.029 |

SOLDERING FOOTPRINT\*



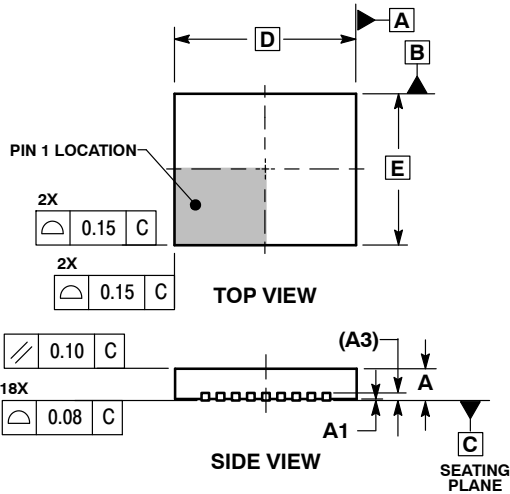
DIMENSIONS: INCHES

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NCP3163, NCV3163

## PACKAGE DIMENSIONS

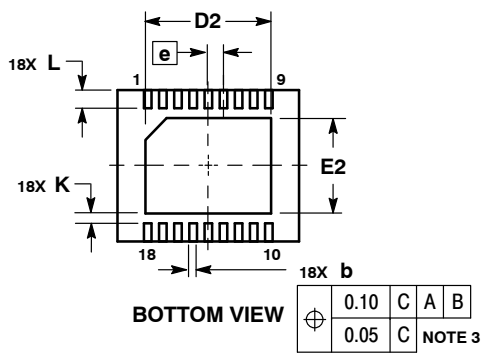
DFN18  
CASE 505-01  
ISSUE D



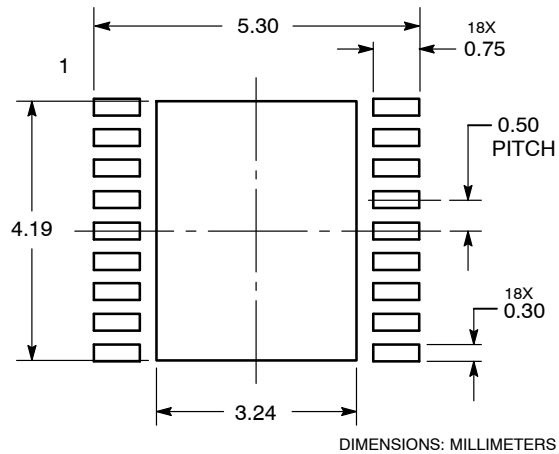
NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS |      |
|-----|-------------|------|
|     | MIN         | MAX  |
| A   | 0.80        | 1.00 |
| A1  | 0.00        | 0.05 |
| A3  | 0.20 REF    |      |
| b   | 0.18        | 0.30 |
| D   | 6.00 BSC    |      |
| D2  | 3.98        | 4.28 |
| E   | 5.00 BSC    |      |
| E2  | 2.98        | 3.28 |
| e   | 0.50 BSC    |      |
| K   | 0.20        | ---  |
| L   | 0.45        | 0.65 |



### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative